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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,935	01/07/2002	Yukihisa Kobayashi	9319S-000319	4909

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,935	KOBAYASHI, YUKIHISA	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,16,21-23,25-32 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,16,21-23,25-32 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/25/05 & 5/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/9/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15, 16, 21-23 and 25-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama (US 6,265,770 B1) in view of Uchiyama et al (US 5,847,796) or vice versa.

As applied to claim 15, Uchiyama teaches a process of mounting a semiconductor component on a substrate (Abstract), comprising:

- a step of mounting a first component (Fig. 1, 2) on a substrate (Fig. 1, 3) by solder connection (Col. 5, lines 20 ff.);

- a step of arranging an anisotropic conductive film (Fig. 1, 4) within a band region (Fig. 1, surround of A) of a surface of the substrate (Cf. Fig. 1, 3);
- a step of arranging a second component (Fig. 1, 6) on the anisotropic conductive film (Fig. 1, 4); and
- a step of thermocompression-bonding (Col. 5, lines 56 ff.) the second component (Fig. 1, 6) to said substrate (Fig. 1, 3) with said anisotropic conductive film (Fig. 1, 4) held therebetween;
- wherein said step of arranging said anisotropic conductive film within said band region of said substrate (Fig. 1, top surface of 3) is performed after said step of mounting the first component on said substrate by the solder connection.

Uchiyama et al teach a method of bonding a driver IC (Fig. 3, 1) with a bonding tool or compression bonding head (Fig. 3, 4), slightly wider than the driver IC but much smaller than a band region or upper surface of the substrate (Fig. 3, 62) in order to have a more uniform load at a more uniform temperature of bonding.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the bonding tool or compression bonding head, as taught by the Uchiyama et al to the IC mounting process of Uchiyama, in order to have a more uniform load at a more uniform temperature of bonding.

As applied to claim 16, Uchiyama teaches a process of mounting a semiconductor component on a substrate, which reads on applicant's claimed invention, except for mounting the

first component (Fig. 1, 2) on the substrate (Fig. 1, 3) by the solder connection such as a reflow treatment.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to solder (Col. 5, lines 20 ff) the connection by reflow treatment, which is well known in order to increase production.

As applied to claim 21, Uchiyama teaches a process of mounting a semiconductor component on a substrate (Abstract), comprising:

a.) selecting a band region of a surface of the substrate (Fig. 1, surround of A) of the circuit board or substrate (Fig. 1, 3);

b.) soldering a first component (Fig. 1, 2; Col. 5, lines 20 ff.) onto the circuit board (Fig. 1, 3) outside of the band region (Fig. 1, surround of A); and

c.) after step b.) where the first component (Fig. 1, 2) is soldered (Fig. 1, 1; Col. 5, lines 20 ff.) to the substrate (Fig. 1, 3), mounting a second component (Fig. 1, 6) on the substrate (Fig. 1, 3) within the band region (Fig. 1, surround of A) with an anisotropic conductive film (Fig. 1, 4).

The '796 teaches a method of bonding a driver IC (Fig. 3, 1) with a bonding tool or compression bonding head (Fig. 3, 4), slightly wider than the driver IC but much smaller than a band region or upper surface of the substrate (Fig. 3, 62) in order to have a more uniform load at a more uniform temperature of bonding.

It would have been obvious to one of ordinary skill in the art at the time the invention

was made to combine the two teachings by applying the bonding tool or compression bonding head, as taught by the '796 to the IC mounting process of Uchiyama, in order to have a more uniform load at a more uniform temperature of bonding.

As applied to claim 22, Uchiyama et al and Uchiyama teach the claimed invention, including the thermal press-bonding (Uchiyama, Col. 5, lines 57 ff.) and a heated bonding head or bonding tool (Uchiyama et al, Fig. 10, 4) pressing against the component (Uchiyama et al, Fig. 10, 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a heated bonding head pressing against the component (Uchiyama et al, Fig. 10, 1) in selected area (Uchiyama, Fig. 1, surround of A) without hitting the first component (Uchiyama, Fig. 1, 2) in order concentrate all the heat toward melting the anisotropic conductive film (Uchiyama, Fig. 1, 4) under the chip (Uchiyama, Fig. 1, 6).

As applied to claims 23 and 28, Uchiyama teaches that the first component (Fig. 1, 2) is selected from the group of passive and mechanical components (Col. 5, lines 15 ff.), and the second component comprises a semiconductor device (Fig. 1, 6; col. 11, line 37) or LCD or power source IC.

As applied to claim 25, Uchiyama teaches the claimed invention, except for providing the alignment marks outside the band region (Fig. 1, surround of A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the alignment marks outside the band region since it was known in the art that reference marks are utilized to assign an exact location of a band region (Fig. 1, A).

As applied to claim 26, Uchiyama teaches that a bonding region by ACF or band region is selected or set aside (Fig. 1, surround of A) when the first components are soldered (Col. 5, lines 20 ff.) to the substrate by conventional technique such as solder reflow.

As applied to claim 27, Uchiyama teaches that the band region (Fig. 1, surround of A) divides a first set of first components (Fig. 1, left set of 2) on one part of the substrate and a second set of first components (Fig. 1, right set of 2) on a second part of the substrate (Fig. 1, 3).

As applied to claim 29, Uchiyama teaches that the band region (Fig. 1, surround of A) can be extended from one end to the other end of the substrate (Fig. 1, 3).

As applied to claim 30, Uchiyama teaches that the band region (Fig. 1, surround of A) extends rectilinearly along the substrate (Fig. 1, 3).

As applied to claim 31, Uchiyama teaches that there are wiring patterns (Fig. 1, 11) on the substrate (Fig. 1, 3) in the band region (Fig. 1, surround of A).

As applied to claim 32, Uchiyama teaches a dummy electrode or ground wire (Fig. 1, 12) at a position associated with the second component or LCD chip (Fig. 1, 6).

As applied to claim 35, Uchiyama teaches a process of mounting a semiconductor component on a substrate (Abstract), comprising:

- a step of mounting a plurality of first components (Fig. 1, 2) within first regions (Fig. 1,

area of 2) on a surface of a substrate (Fig. 1, 3) by a solder connection (Col. 5, lines 20-25);

- a step of arranging an anisotropic conductive film (Fig. 1, 4) on a predetermined position of the substrate (Fig. 1, 3);
- a step of arranging a second component (Fig. 1, 6) on the anisotropic conductive film (Fig. 1, 4);
- a step of thermocompression-bonding (Col. 5, lines 56-60) the second component (Fig. 1, 6) to the substrate (Fig. 1, 3) with the anisotropic conductive film (Fig. 1, 4) held therebetween;
- wherein the step of arranging the anisotropic conductive film on the predetermined position of the substrate is performed (Fig. 1, 1) after said step of mounting the first component on said substrate by the solder connection;
- the substrate includes a band region (Fig. 1, surround of A) that extends between the first regions; and
- the band region includes the second component (Fig. 1, 6) other than the first component (Fig. 1, 2).

Uchiyama et al teach a method of bonding a driver IC (Fig. 3, 1) with a bonding tool or compression bonding head (Fig. 3, 4), slightly wider than the driver IC but much smaller than a band region or upper surface of the substrate (Fig. 3, 62) in order to have a more uniform load at a more uniform temperature of bonding.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the bonding tool or compression bonding head along the surface including its longitudinal one of a component, as taught by the Uchiyama et al to the IC mounting process of Uchiyama, in order to have a more uniform load at a more uniform temperature of bonding at the band region where the anisotropic film (Uchiyama ; Fig. 1, 4) is arranged.

Response to Arguments

4. Applicant's arguments filed 8/09/0 have been fully considered but they are not persuasive for the following reasons:

Applicant urges *inter alia* that Uchiyama does not teach a bonding head narrower than a band region (Remarks, page 8, 1st paragraph; page 9, 2nd paragraph. The examiner's position, as stated in the previous action, is and continues to be that since Uchiyama teaches the band region as the surface area (Fig. 1, 2) of the substrate (Fig. 3, 62), which is much wider than the component (Fig. 3, 1) and the comparative bonding head (Fig. 3, 4).

Applicant's arguments (Remarks, page 8, 2ns paragr. – page 9, 1st paragr.) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Moreover Uchiyama teaches the soldering of electronic

chips (Fig. 1, 2; col. 5, lines 20-25) then the heat press-bonding of the second component (Fig. 1, 6; col. 5, lines 50-60).

Applicants' arguments with respect to claim 35 have been considered but are moot in view of the new grounds of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application lnformation Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CARL J. ARBES
PRIMARY EXAMINER

Tim Phan
Examiner
Art Unit 3729

tp
August 21, 2005